CLAIMS

1. An apparatus comprising:

an array of memory cells;

a refresh circuit configured to refresh said array in response to a refresh control signal;

a first monitor cell configured to have a charge leakage similar to said memory cells;

a second monitor cell configured to have a discharge leakage similar to said memory cells;

a control circuit configured to generate said refresh control signal in response to either a voltage level of said first monitor cell rising above a first pre-determined threshold level or a voltage level of said second monitor cell dropping below a second pre-determined threshold level, wherein said first and said second threshold levels are different.

2. The apparatus according to claim 1, wherein said control circuit comprises:

a first comparator circuit configured to generate a first control signal in response to said voltage level of said first

monitor cell rising above said first pre-determined threshold level;

a second comparator circuit configured to generate a second control signal in response to said voltage level of said second monitor cell rising above said second pre-determined threshold level; and

a logic circuit configured to generate said refresh control signal in response to said first and said second control signals.

3. The apparatus according to claim 2, wherein said logic circuit comprises a one-shot circuit configured to generate said refresh control signal having a predetermined pulse width.

4. The apparatus according to claim 1, wherein said control circuit is configured to operate with both symmetrical and asymmetrical charge and discharge leakages.

5. The apparatus according to claim 1, wherein said first monitor cell and said second monitor cell comprise memory cells that are structurally similar to memory cells of said array.

6. The apparatus according to claim 5, wherein said monitor cells are configured to have a similar environment to said memory cells of said array.

7. The apparatus according to claim 6, wherein a bitline of said first monitor cell and a bitline of said second monitor cell are set to an equalization potential of said array during a monitoring operation.

8. The apparatus according to claim 1, further comprising:

a plurality of monitor cells configured to have a charge leakage similar to said memory cells;

a plurality of monitor cells configured to have a discharge leakage similar to said memory cells, wherein said control circuit is further configured to generate said refresh control signal in response to any of said monitor cells exceeding a respective one of said first pre-determined threshold level or said second pre-determined threshold level.

9. The apparatus according to claim 1, wherein said first monitor cell and said second monitor cell comprise memory cells of said array.

10. The apparatus according to claim 1, wherein said array of memory cells comprises 1T memory cells.

11. The apparatus according to claim 1, further comprising a sense amplifier configured to program said first monitor cell with a first binary value and said second monitor cell with a second binary value in response to said refresh control signal.

12. An apparatus for controlling a refresh of a memory array comprising:

means for monitoring a charge leakage of an array of memory cells;

means for monitoring a discharge leakage of an array of memory cells; and

means for generating a refresh control signal in response to either a voltage level of said first monitoring means rising

above a first pre-determined threshold level or a voltage level of said second monitoring means dropping below a second pre-determined threshold level, wherein said first and second threshold levels are different.

13. A method for controlling a refresh operation of a memory array comprising the steps of:

monitoring a charge leakage of a first monitor cell;

monitoring a discharge leakage of a second monitor cell; and

generating a refresh control signal in response to either a voltage level of said first monitor cell rising above a first pre-determined threshold level or a voltage level of said second monitor cell dropping below a second pre-determined threshold level, wherein said first and second pre-determined threshold levels are different.

14. The method according to claim 13, further comprising the steps of:

programming said first monitor cell with a first binary value; and

programming said second monitor cell with a complement of said first binary value.

15. The method according to claim 13, further comprising the step of:

equalizing a bitline voltage level of said first monitor cell and a bitline voltage level of said second monitor cell with a bitline equalization voltage level of said memory array.

16. The method according to claim 13, further comprising the steps of:

generating a first control signal in response to a comparison of a voltage level of said first monitor cell to said first pre-determined threshold level; and

generating a second control signal in response to a comparison of a voltage level of said second monitor cell to said second pre-determined threshold level.

17. The method according to claim 13, further comprising the step of:

generating said refresh control signal having a predetermined pulse width.

18. The method according to claim 13, further comprising the step of:

selecting said first and said second predetermined threshold levels to provide a margin between a refresh operation and a loss of retention.

19. The method according to claim 18, wherein said first and said second predetermined thresholds are selected to balance maximizing a period between refresh operations and providing said margin.

20. The method according to claim 13, Further comprising the step of:

refreshing a first stored value of said first monitor cell and a second stored value of said second monitor cell in response to said refresh control signal.